OIPE JC105
JUL 22 2004
PATENT & TRADEMARK OFFICE

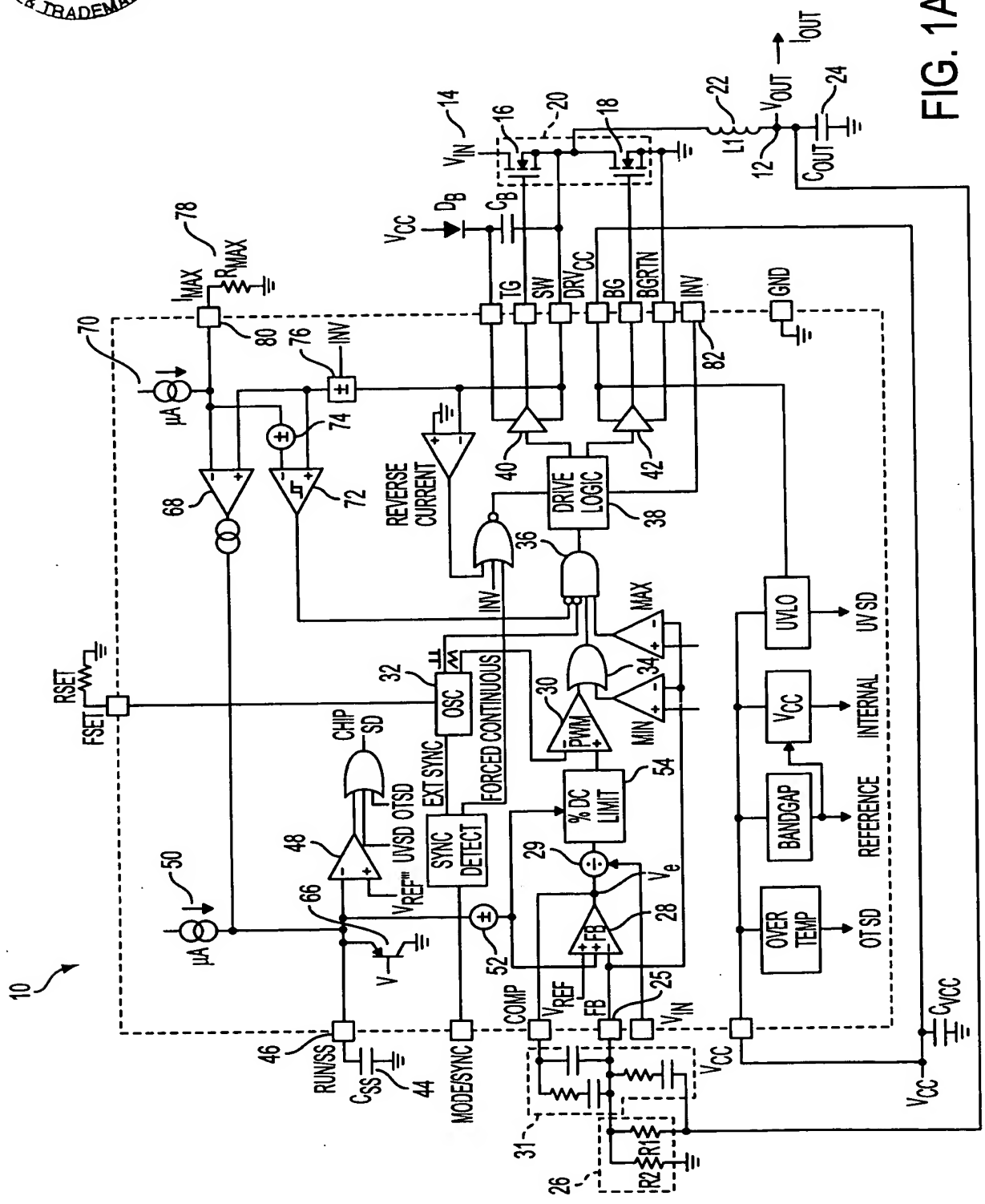

FIG. 1A

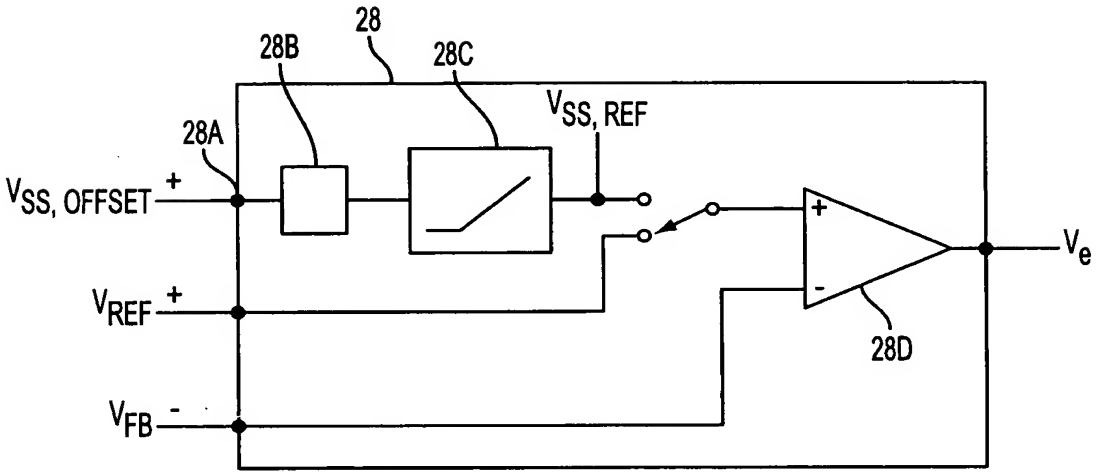

FIG. 1B

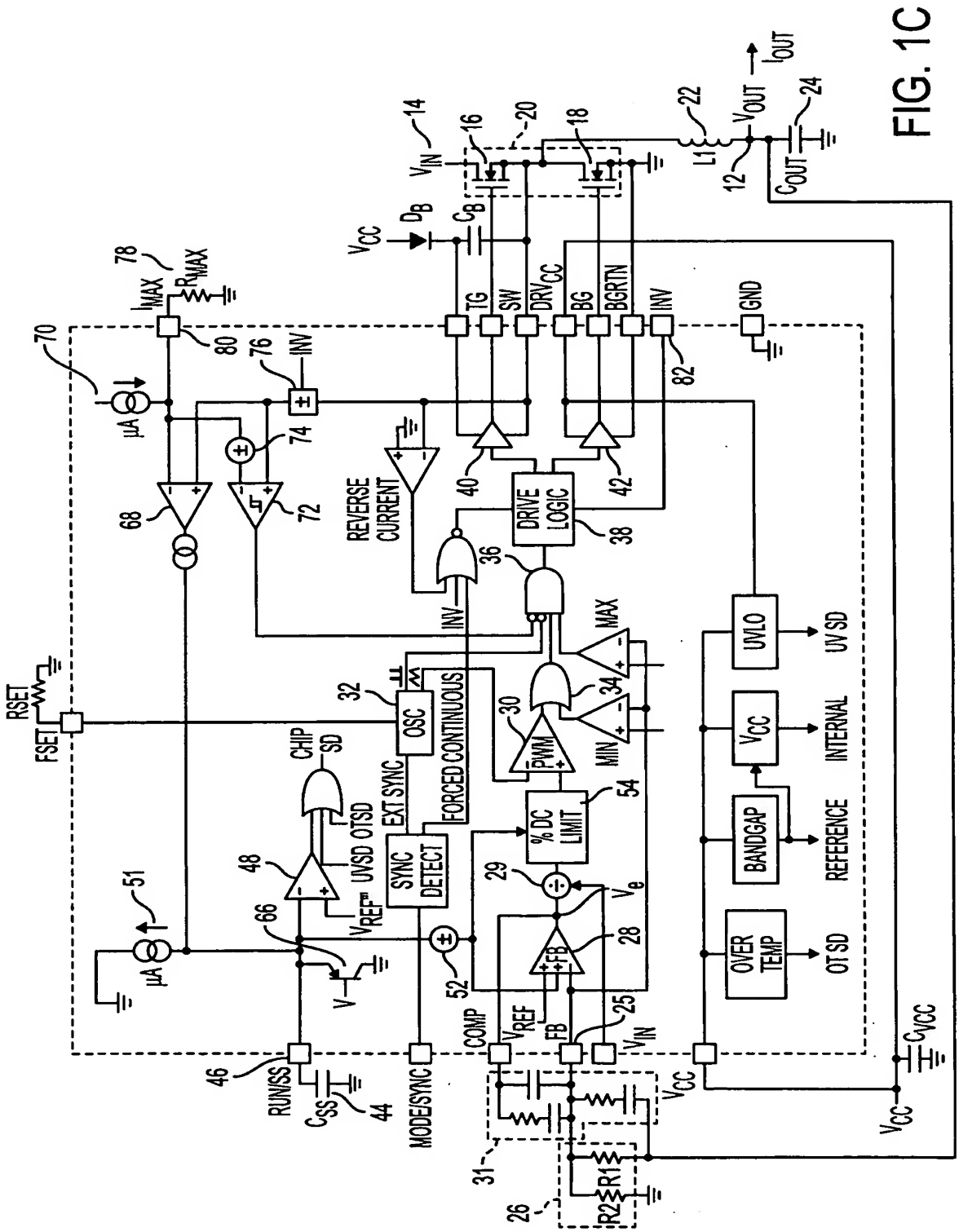
VIN
VCC
DB
CB
TG
SW
DRVCC
BG
BGRTN
INV
GND
L1
VOUT
IOUT
COUT
IMAX
RMAX
μA
REVERSE CURRENT
DRIVE LOGIC
MAX
MIN
PWM
OSC
FORCED CONTINUOUS
EXT SYNC
CHIP SD
UVSD OTSD
SYNC DETECT
% DC LIMIT
VREF
VC
FB
COMP
RUN/SS
CSS
MODE/SYNC
RSET
FSET
UVLO
UV SD
INTERNAL
BANDGAP
REFERENCE
OVER TEMP
OT SD
CVCC
R1
R2

FIG. 1C

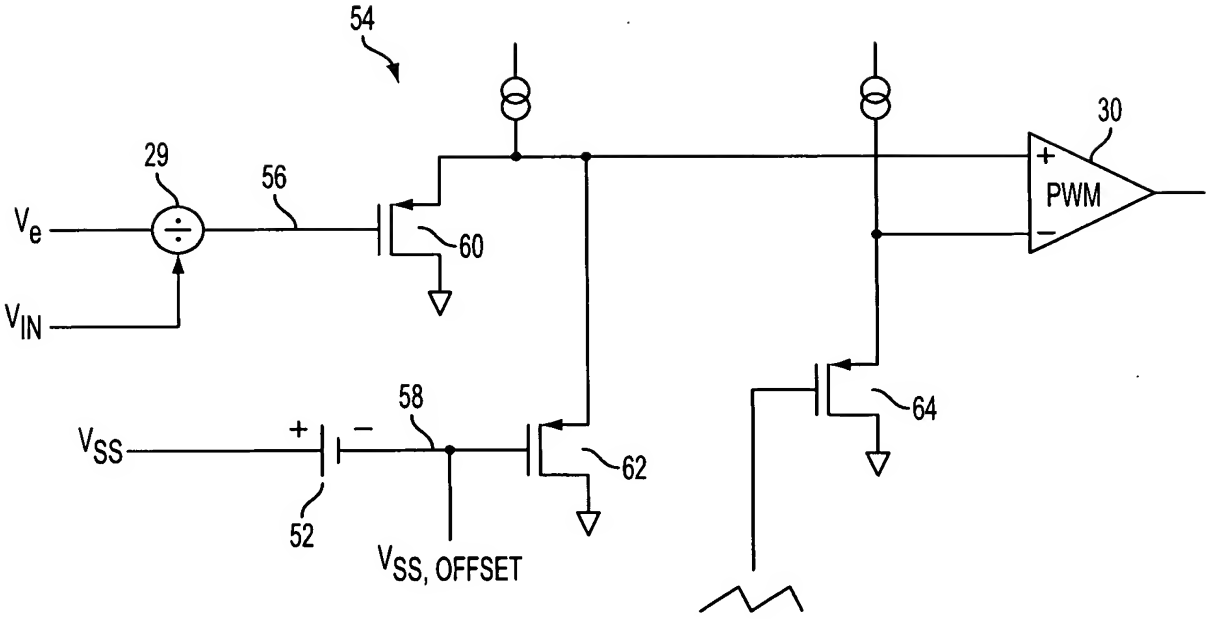

FIG. 2

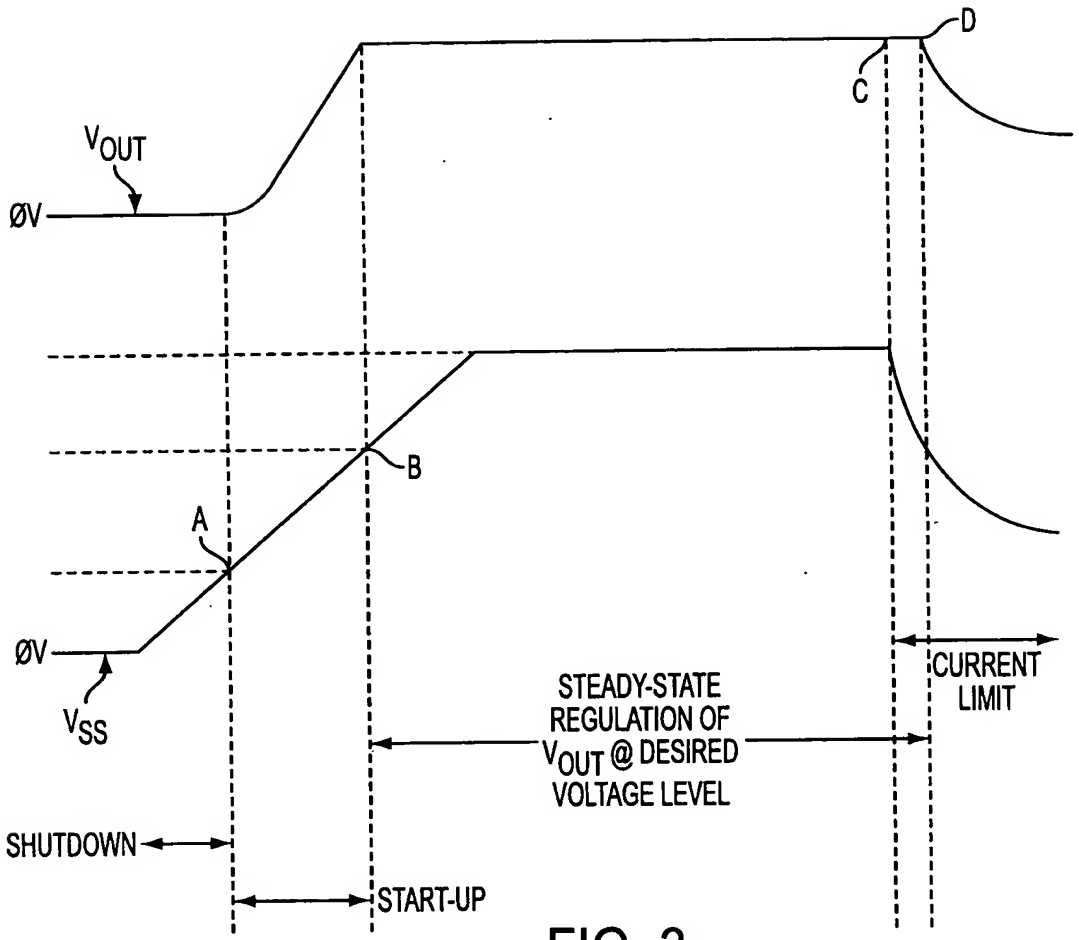
D
C
V_{OUT}
ØV
B
A
ØV
V_{SS}
CURRENT LIMIT
STEADY-STATE REGULATION OF V_{OUT} @ DESIRED VOLTAGE LEVEL
SHUTDOWN
START-UP

FIG. 3

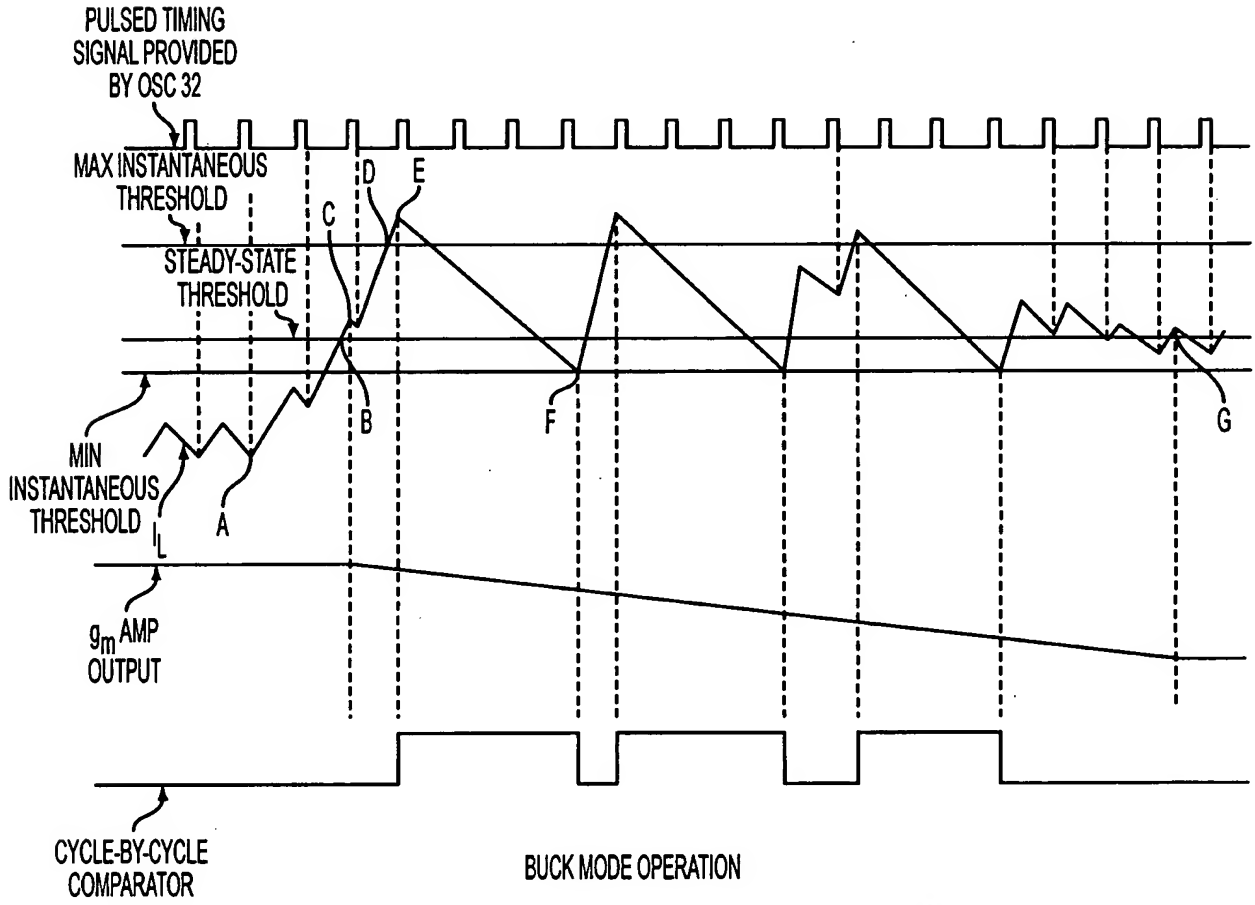
PULSED TIMING SIGNAL PROVIDED BY OSC 32
MAX INSTANTANEOUS THRESHOLD
STEADY-STATE THRESHOLD
MIN INSTANTANEOUS THRESHOLD
I_L
g_m AMP OUTPUT
CYCLE-BY-CYCLE COMPARATOR
A
B
C
D
E
F
G
BUCK MODE OPERATION

FIG. 4

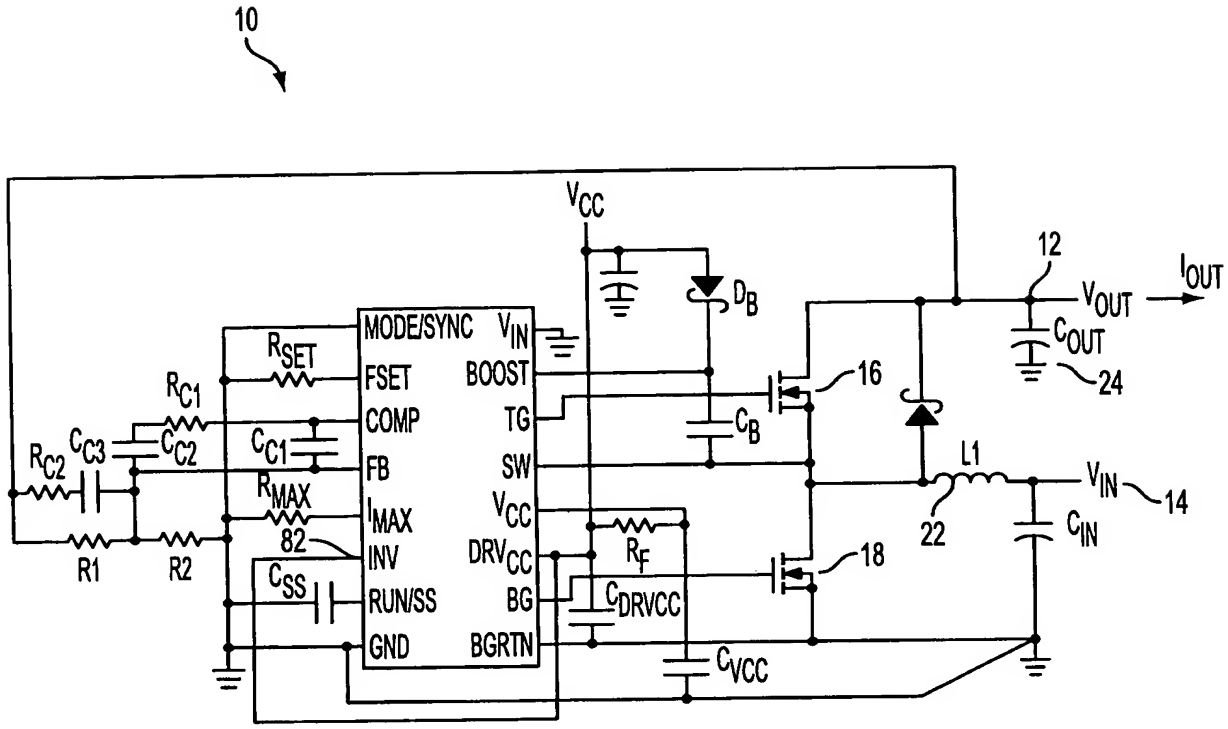
10
VCC
DB
12
IOUT
VOUT
COUT
24
MODE/SYNC
VIN
RSET
FSET
BOOST
16
RC1
COMP
TG
CB
CC3
CC2
CC1
RC2
FB
SW
L1
VIN
14
RMAX
IMAX
VCC
22
CIN
82
INV
DRVCC
RF
18
R1
R2
CSS
RUN/SS
BG
CDRVCC
GND
BGRTN
CVCC

FIG. 5

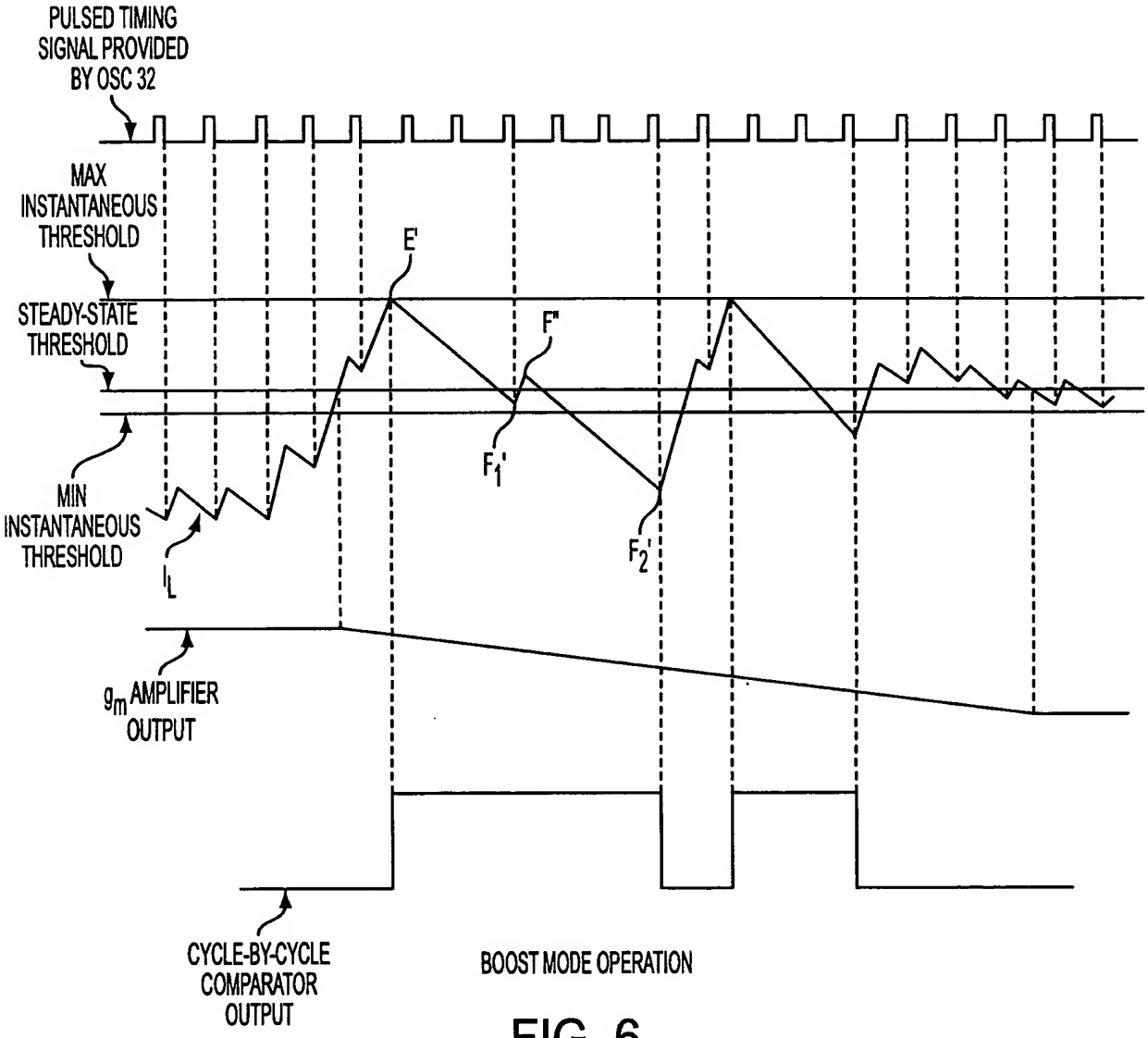
PULSED TIMING SIGNAL PROVIDED BY OSC 32
MAX INSTANTANEOUS THRESHOLD
STEADY-STATE THRESHOLD
MIN INSTANTANEOUS THRESHOLD
E'
F"
F1'
F2'
IL
gm AMPLIFIER OUTPUT
CYCLE-BY-CYCLE COMPARATOR OUTPUT
BOOST MODE OPERATION

FIG. 6

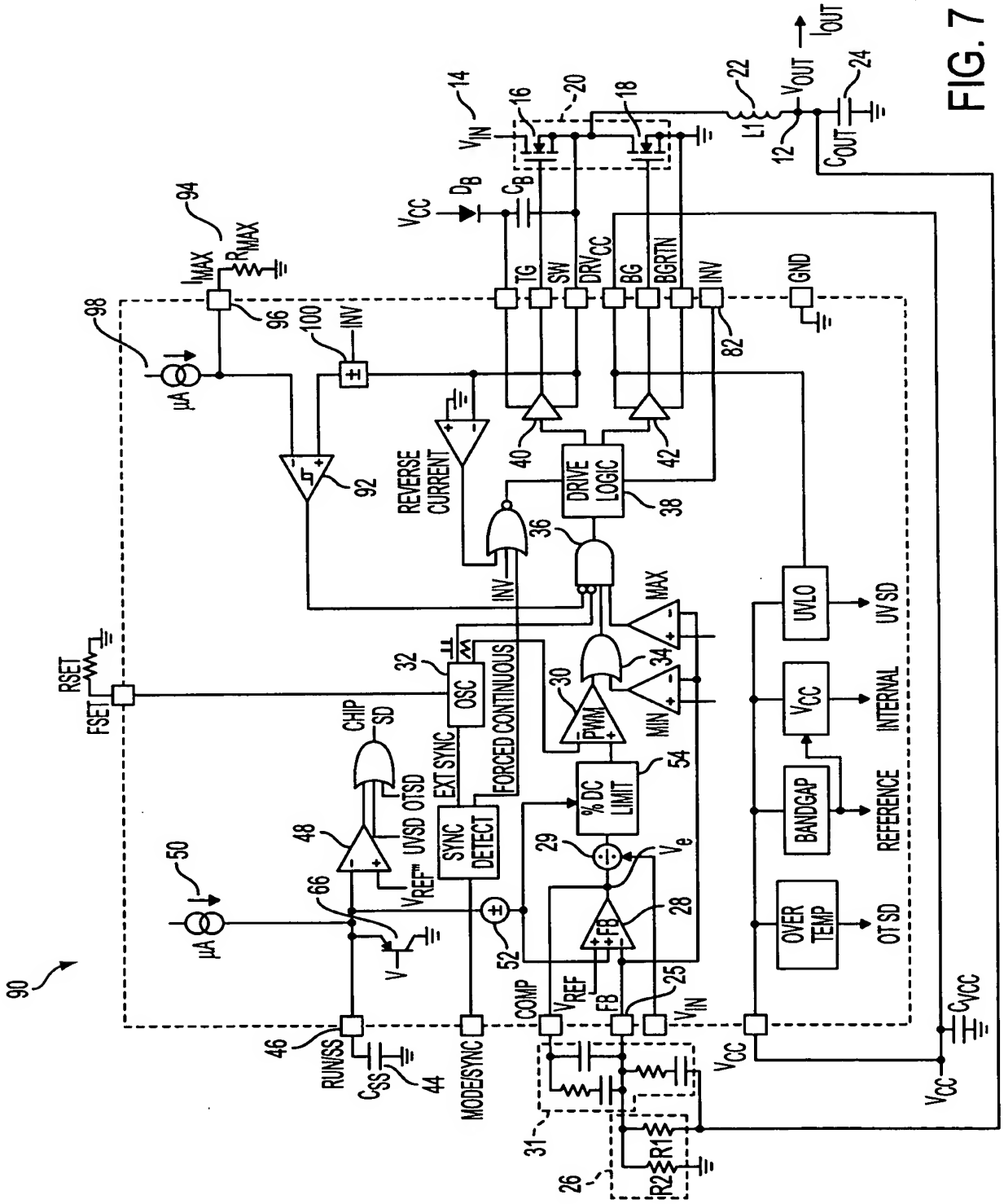
90
VIN
14
16
20
18
22
L1
VOUT
IOUT
24
COUT
12
VCC
DB
CB
94
IMAX
RMAX
98
96
100
INV
TG
SW
DRVCC
BG
BGRTN
INV
GND
82
µA
92
REVERSE CURRENT
40
42
DRIVE LOGIC
38
36
INV
MAX
MIN
RSET
FSET
32
OSC
FORCED CONTINUOUS
30
PWM
34
CHIP SD
EXT SYNC
UVSD OTSD
SYNC DETECT
% DC LIMIT
54
48
50
µA
66
VREF
29
Ve
28
FB
52
V
COMP
VREF
FB
25
VIN
UVLO
UVSD
VCC
INTERNAL
BANDGAP
REFERENCE
OVER TEMP
OTSD
CVCC
VCC
VCC
46
RUN/SS
CSS
44
MODE/SYNC
31
R1
R2
26

FIG. 7